CLAIMS

1. A method of storing, in a circuit, information concerning a condition of a fuse; said method comprising:

supplying a first signal to said circuit which sets said circuit in a first state when said fuse is in a first condition and keeps said circuit unchanged when said fuse is in a second condition; and

supplying a second signal to said circuit, while said first signal is being supplied, that keeps said circuit in said first state when said fuse is in said first condition and sets said circuit in a second state when said fuse is in said second condition.

2. The method of claim 1 wherein said fuse is in said first condition when said fuse is intact, and said fuse is in said second condition when said fuse is blown.

3. The method of claim 1 wherein said first signal comprises a strobe signal.

4. The method of claim 1 wherein said second signal comprises a pre-charge signal.

5. The method of claim 1 wherein said first state comprises a lower voltage and said second state comprises a higher voltage.

6. The method of claim 1 further comprising terminating said first signal and said second signal concurrently.

7. A method of correcting an error in information stored in a circuit concerning a condition of a fuse; said method comprising:

supplying a first signal to said circuit which sets said circuit in a first state when said fuse is in a first condition and keeps said circuit unchanged when said fuse is in a second condition; and

supplying a second signal to said circuit, while said first signal is being supplied, that keeps said circuit in said first state when said fuse is in said first condition

and sets said circuit in a second state when said fuse is in said second condition.

8. The method of claim 7 wherein said fuse is in said first condition when said fuse is intact, and said fuse is in said second condition when said fuse is blown.

9. The method of claim 7 wherein said first signal comprises a strobe signal.

10. The method of claim 7 wherein said second signal comprises a pre-charge signal.

11. The method of claim 7 wherein said first state comprises a lower voltage and said second state comprises a higher voltage.

12. The method of claim 7 further comprising terminating said first signal and said second signal concurrently.

13. A method of storing, in a latch circuit, information concerning a condition of a fuse; said latch circuit comprising a pair of inverter circuits, a first transistor, and a second transistor; said pair of inverter circuits being connected in anti-parallel with a common input terminal and a common output terminal; said first transistor having a first terminal coupled to said input terminal of said pair of inverter circuits, a further terminal coupled to a further terminal of said fuse, and a gate terminal coupled to a strobe line; and said second transistor having a first terminal coupled to a supply voltage, a further terminal coupled to said further terminal of said fuse and to said further terminal of said first transistor, and a gate terminal coupled to a pre-charge line; said method comprising:

supplying a first signal on said strobe line that activates said first transistor thereby setting said input terminal of said pair of inverter circuits at a first voltage state when said fuse is in a first condition and keeping a voltage state of said input terminal of said pair of inverter circuits unchanged when said fuse is in a second condition; and

supplying a second signal on said pre-charge line while said first signal is being supplied on said strobe line, said second signal activating said second transistor thereby keeping said input terminal of said pair of inverter circuits in said first voltage state when said fuse is in said first condition and setting said input terminal of said pair of inverter circuits at a second voltage state when said fuse is in said second condition.

14. The method of claim 13 wherein said fuse is in said first condition when said fuse is intact, and said fuse is in said second condition when said fuse is blown.

15. The method of claim 13 wherein said first signal is initiated by a change from a lower voltage to a higher voltage, and said first transistor is an n-channel transistor.

16. The method of claim 13 wherein said second signal is initiated by a change from a higher voltage to a lower voltage, and said second transistor is a p-channel transistor.

17. The method of claim 13 wherein said first voltage state comprises a lower voltage and said second voltage state comprises a higher voltage.

18. The method of claim 13 further comprising terminating said first signal and said second signal concurrently.

19. A method of correcting an error in information stored in a latch circuit concerning a condition of a fuse; said latch circuit comprising a pair of inverter circuits, a first transistor, and a second transistor; said pair of inverter circuits being connected in anti-parallel with a common input terminal and a common output terminal; said first transistor having a first terminal coupled to said input terminal of said pair of inverter circuits, a further terminal coupled to a further terminal of said fuse, and a gate terminal coupled to a strobe line; and said second transistor having a first terminal coupled to a supply voltage, a further

terminal coupled to said further terminal of said fuse and to said further terminal of said first transistor, and a gate terminal coupled to a pre-charge line; said method comprising:

supplying a first signal on said strobe line that activates said first transistor thereby setting said input terminal of said pair of inverter circuits at a first voltage state when said fuse is in a first condition and keeping a voltage state of said input terminal of said pair of inverter circuits unchanged when said fuse is in a second condition; and

supplying a second signal on said pre-charge line while said first signal is being supplied on said strobe line, said second signal activating said second transistor thereby keeping said input terminal of said pair of inverter circuits in said first voltage state when said fuse is in said first condition and setting said input terminal of said pair of inverter circuits at a second voltage state when said fuse is in said second condition.

20. The method of claim 19 wherein said fuse is in said first condition when said fuse is intact, and said fuse is in said second condition when said fuse is blown.

21. The method of claim 19 wherein said first signal is initiated by a change from a lower voltage to a higher voltage, and said first transistor is an n-channel transistor.

22. The method of claim 19 wherein said second signal is initiated by a change from a higher voltage to a lower voltage, and said second transistor is a p-channel transistor.

23. The method of claim 19 wherein said first voltage state comprises a lower voltage and said second voltage state comprises a higher voltage.

24. The method of claim 19 further comprising terminating said first signal and said second signal concurrently.

25. A circuit comprising:

a device operable to remain in one of at least a first state and a second state;

a first input operable to receive a first signal which sets said device in said first state when a fuse is in a first condition and keeps a state of said device unchanged when said fuse is in a second condition; and

a second input operable to receive a second signal, while said first signal is being supplied to said first input, that keeps said device in said first state when said fuse is in said first condition and sets said device in said second state when said fuse is in said second condition.

26. The circuit of claim 25 wherein said fuse is in said first condition when said fuse is intact, and said fuse is in said second condition when said fuse is blown.

27. The circuit of claim 25 wherein said device comprises a pair of inverter circuits connected in an anti-parallel arrangement and with a common input terminal and a common output terminal.

28. The circuit of claim 25 wherein said first input comprises an n-channel transistor having a first terminal coupled to an input terminal of said device, a further terminal coupled to a further terminal of said fuse, and a gate terminal coupled to a strobe line

29. The circuit of claim 25 wherein said second input comprises a p-channel transistor having a first terminal coupled to a supply voltage, a further terminal coupled to a further terminal of said fuse, and a gate terminal coupled to a pre-charge line.

30. The circuit of claim 25 wherein said first state comprises a lower voltage and said second state comprises a higher voltage.

31. The circuit of claim 25 wherein said first signal comprises a strobe signal.

32. The circuit of claim 25 wherein said second signal comprises a pre-charge signal.

33. A latch circuit for reading, holding and outputting information concerning a condition of a fuse, said fuse having a first terminal coupled to a ground potential, said circuit comprising:

a pair of inverter circuits connected in an anti-parallel arrangement and with a common input terminal and a common output terminal;

a first transistor having a first terminal coupled to said input terminal of said pair of inverter circuits, a further terminal coupled to a further terminal of said fuse, and a gate terminal coupled to a first signal line; and

a second transistor having a first terminal coupled to a supply voltage, a further terminal coupled to said further terminal of said fuse and to said further terminal of said first transistor, and a gate terminal coupled to a second signal line;

said first transistor, when activated by a first signal delivered by said first signal line, setting said input terminal of said pair of inverter circuits at a first voltage when said fuse is in a first condition and keeping a voltage state of said input terminal of said pair of inverter circuits unchanged when said fuse is in a second condition;

said second transistor, when activated by a second signal delivered by said second signal line while said first signal is being delivered by said first signal line, keeping said input terminal of said pair of inverter circuits at said first voltage when said fuse is in a first condition and setting said input terminal of said pair of inverter circuits at a second voltage when said fuse is in a second condition.

34. The latch circuit of claim 33 wherein said fuse is in said first condition when said fuse is intact, and said fuse is in said second condition when said fuse is blown.

35. The latch circuit of claim 33 wherein said first state comprises a lower voltage and said second state comprises a higher voltage.

36. The latch circuit of claim 33 wherein said first signal line comprises a strobe signal line.

37. The latch circuit of claim 33 wherein said second signal line comprises a pre-charge signal line.